In the Claims:

Please cancel Claim 1 and please add new Claims 2-23, as shown below.

2. (New) A method for designing a derivative circuit block, comprising:

(a) selecting a original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the circuit design;

(c) planning a chip layout;

(d) programming at least one of the one or more programmable fabrics; and

(e) performing verification of the derivative circuit block.

3. (New) The method of claim 2, wherein the step of planning the chip layout does not result in altering the chip layout.

4. (New) The method of claim 2, further comprising the step of performing clocking and timing analysis prior to the step of performing verification of the derivative circuit block.

5. (New) The method of claim 2, further comprising the step of performing power analysis prior to the step of performing verification of the derivative circuit block.

6. (New) The method of claim 2, wherein only a set of new functionality added the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

7. (New) The method of claim 2, wherein step A through step E are repeated to design a second derivative design, such that the original circuit design of the second derivative design is a derivative design.

8. (New) The method of claim 2, wherein the step of planning the chip layout comprises:

analyzing timing requirements to ensure the derivative circuit block meets all applicable timing requirements.

9. (New) The method of claim 2, further comprising the step of assembling the chip prior to the step of performing verification of the derivative circuit block.

10. (New) The method of claim 2, wherein the original circuit design further comprises one or more non-programmable fabrics.

11. (New) The method of claim 10, wherein the one or more programmable fabrics each has a port access and hierarchical routing.

12. (New) The method of claim 10, further comprising the step of determining a power level for each programmable fabric and each non-programmable fabric through simulation.

13. (New) A computer readable medium carrying one or more sequences of one or more instructions for designing a derivative circuit block, wherein the execution of the one or more sequences of the one or more instructions causes the one or more processors to perform the steps of:

(b) selecting a original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the circuit design;

(c) planning a chip layout;

(d) programming at least one of the one or more programmable fabrics; and

(e) performing verification of the derivative circuit block.

14. (New) The computer readable medium of claim 13, wherein the step of planning the chip layout does not result in altering the chip layout.

15. (New) The computer readable medium of claim 13, further comprising the step of performing clocking and timing analysis prior to the step of performing verification of the derivative circuit block.

16. (New) The computer readable medium of claim 13, further comprising the step of performing power analysis prior to the step of performing verification of the derivative circuit block.

17. (New) The computer readable medium of claim 13, wherein only a set of new functionality added the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

18. (New) The computer readable medium of claim 13, wherein step A through step E are repeated to design a second derivative design, such that the original circuit design of the second derivative design is a derivative design.

19. (New) The computer readable medium of claim 13, wherein the step of planning the chip layout comprises:

analyzing timing requirements to ensure the derivative circuit block meets all applicable timing requirements.

20. (New) The computer readable medium of claim 13, further comprising the step of assembling the chip prior to the step of performing verification of the derivative circuit block.

21. (New) The computer readable medium of claim 13, wherein the original circuit design further comprises one or more non-programmable fabrics.

22. (New) The computer readable medium of claim 21, wherein the one or more programmable fabrics each has a port access and hierarchical routing.

23. (New) The computer readable medium of claim 21, further comprising the step of determining a power level for each programmable fabric and each non-programmable fabric through simulation.